AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraphs in the original filed specification beginning at page 5, line 3, and ending at page 12, line 27, which previously had been replaced (up to page 12, line 18) as noted in the June 9, 2005 Amendment at pages 3-11, with the following new paragraphs:

The present invention provides a constant voltage generating circuit comprising a plurality of first pnp transistors including n (an integer; $2 \leq n$) first pnp transistors, a collector of each of the plurality of first pnp transistors being grounded, a base of a first one of the plurality of first pnp transistors being grounded, a base of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first pnp transistors being connected to an emitter of a (k-1)-th one of the plurality of first pnp transistors; a plurality of second pnp transistors including n second pnp transistors, each having an emitter area greater than that of each of the plurality of first pnp transistors, a collector of each of the plurality of second pnp transistors being grounded, a base of a first one of the plurality of second pnp transistors being grounded, a base of a k-th one of the plurality of second pnp transistors, except for another one of the plurality of second pnp transistors, being connected to an emitter of a (k-1)-th one of the plurality of second pnp transistors; primary current sources connected to the respective emitters of said plurality of first pnp transistors and the respective emitters of said plurality of second pnp transistors, except for an emitter of the first one of the plurality of second pnp transistors, to supply currents to the respective pnp transistors of said pluralities of first and second pnp transistors, two resistors being connected in series between the emitter of said first one of the

plurality of second pnp transistors and the corresponding primary current source, a connection point between the two resistors being connected to the base of said another one of the plurality of second pnp transistors; and current control means including a first input terminal to which the emitter of a n-th one of the plurality of first pnp transistors is connected and a second input terminal to which the emitter of a n-th one of the plurality of second pnp transistors is connected, the current control means controlling currents from the primary current sources by outputting a control signal that controls the currents from said primary current sources so that a potential at said first input terminal and a potential at said second input terminal are the same.

The present invention also provides a constant voltage generating circuit comprising a plurality of first npn transistors including n (an integer; $2 \leq n$) first npn transistors, a base and a collector of each of the plurality of first npn transistors being connected together, an emitter of a first one of the plurality of first npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of first npn transistors being connected to a collector of a (k-1)-th one of the plurality of first npn transistors; a plurality of second npn transistors including n second npn transistors, each having an emitter area greater than that of each of the plurality of first npn transistors, a base and a collector of each of said plurality of second npn transistors being connected together, an emitter of a first one of the plurality of second npn transistors being grounded, an emitter of a k (an integer; $2 \leq k \leq n$)-th one of the plurality of second npn transistors, except another one of the plurality of second npn transistors, being connected to a collector of a (k-1)-th one of the plurality of second npn transistors; primary current sources connected respectively to the collector of a n-th one of said

plurality of first npn transistors and to the collector of a n-th one of the plurality of second npn transistors to supply currents to the respective npn transistors of the pluralities of first and second npn transistors, said first one of the plurality of second npn transistors being connected to a corresponding primary current source via two resistors connected in series, a connection point between the two resistors being connected to an emitter of said another one of the plurality of second npn transistors; and current control means including a first input terminal to which the collector of said n-th one of the plurality of first npn transistors is connected and a second input terminal to which the collector of said n-th one of the plurality of second npn transistors is connected, the current control means controlling currents from said primary current sources by outputting a control signal that controls the currents from said primary current sources so that a potential at the first input terminal and a potential at the second input terminal are the same.

The present invention also provides a constant voltage generating circuit wherein said current control means further comprises a differential voltage generating means which includes a differential amplifier including said first input terminal and said second input terminal and outputting said control signal, and an offset voltage at said differential amplifier in input equivalent has a primary temperature characteristic.

The present invention also provides a constant voltage generating circuit wherein said current control means comprises a differential amplifier including: at least one first bipolar transistor of a first polarity, having a collector, emitter, and base; at least one second bipolar transistor of said first polarity, having a collector, emitter, and base, said second bipolar transistor having an emitter area larger than that of said first bipolar

transistor; the emitter-collector path of said first bipolar transistor being connected in series between a first secondary current source and a node, and said base forming said first input terminal of said current control means; and the emitter-collector path of said second bipolar transistor being connected in series between a second secondary current source and said node, with the connection to said secondary current source providing said control signal that controls said current for said primary current sources, and said base forming said second input terminal of said current control means.

The present invention also provides a constant voltage generating means wherein there are a plurality m of additional first bipolar transistors with their emitter-collector paths connected in series between the at least one first bipolar transistor and said node, and with the base of each connected to the side of the emitter-collector path of that transistor farthest from said node, and a plurality m of additional second bipolar transistors with their emitter-collector paths connected in series between the at least one second bipolar transistor and said node, and with the base of each connected to the side of the emitter-collector path of that transistor farthest from said node.

The present invention also provides a constant voltage generating circuit wherein said current control means further comprises a differential amplifier having a differential pair including a first npn differential pair transistor and a second npn differential pair transistor having an emitter area larger than that of the first npn differential pair transistor, and another current source that supplies a current to said differential pair; wherein said differential pair includes said first and second input terminals, said first input terminal is a base of said first npn differential pair transistor and said second input terminal is a base of said second npn differential pair transistor, and wherein a collector

of said first npn differential pair transistor is connected to said another current source, and a collector of said second differential pair npn transistor is connected to said another current source.

The present invention also provides a constant voltage generating circuit wherein said current control means further comprises a differential amplifier having a differential pair including a first npn differential pair transistor, a second npn differential pair transistor having an emitter area greater than that of the first npn differential pair transistor, first and second secondary current sources to supply current to said differential pair, and said differential amplifier has a plurality of third npn differential pair transistors including m (an integer; $1 \leq m$) third npn differential pair transistors, and a plurality of fourth npn differential pair transistors including m fourth npn differential pair transistors each having an emitter area greater than that of the m third npn differential pair transistors; wherein said differential pair includes said first and second input terminals, said first input terminal being a base of said first npn differential pair transistor, and said second input terminal being a base of said second npn differential pair transistor; and wherein a collector of said first npn differential pair transistor is connected to said first secondary current source, and a collector of said second npn differential pair transistor is connected to said second secondary current source; wherein a base and a collector of each of said pluralities of third npn differential pair transistors are connected together, an emitter of a k (an integer; $2 \leq k \leq m$)-th one of the plurality of third npn differential pair transistors is connected to a collector of a (k-1)-th one of the plurality of third npn differential pair transistors, and the collector of a first one of said plurality of third npn differential pair transistors is connected to the emitter of the

first npn differential pair transistor constituting said differential pair; and wherein a base and a collector of each of said plurality of fourth npn differential pair transistors are connected together, an emitter of a k (an integer; $2 \leq k \leq m$)-th one of the plurality of fourth npn differential pair transistors is connected to a collector of a (k-1)-th one of the plurality of fourth npn differential pair transistors, the collector of a first one of said plurality of fourth npn differential pair transistors is connected to the emitter of the second npn differential pair transistor constituting the differential pair, and the emitter of an m-th one of said plurality of fourth npn transistors is connected to the emitter of an m-th one of said plurality of third npn differential pair transistors.